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Section: A

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Project A

outputs of main control:

o\_reg\_dest; -- ‘1’ write to rd, ‘0’ will not

o\_jump; -- ‘1’jump flag as selector of 2 to 1 mux, ‘0’ select 0 value

o\_branch; -- ‘1’jump flag as selector of 2 to 1 mux, ‘0’ select 0 value, will and with ALU zero flag

o\_mem\_to\_reg; -- write ALU output to reg file or not

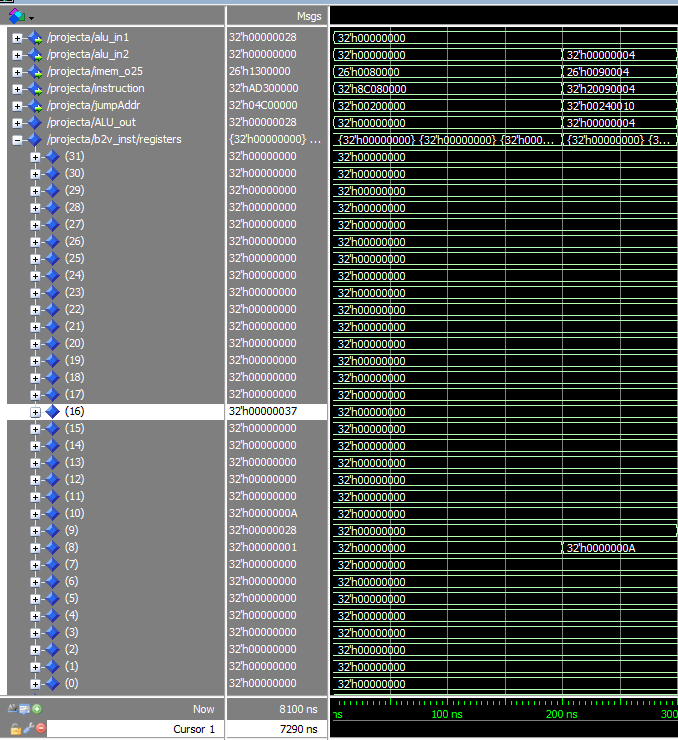
o\_ALU\_op; -- operation code in ALU

o\_mem\_write; -- write to memory or not

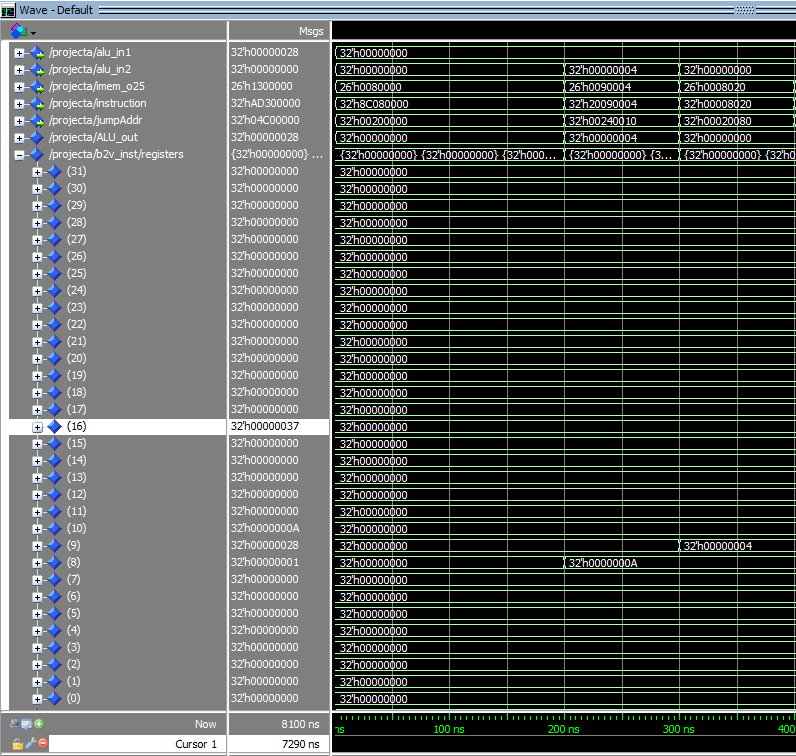
o\_ALU\_src; -- select immidiate data as second input to ALU or rt data

o\_reg\_write; -- write enable to write register file (write rd)

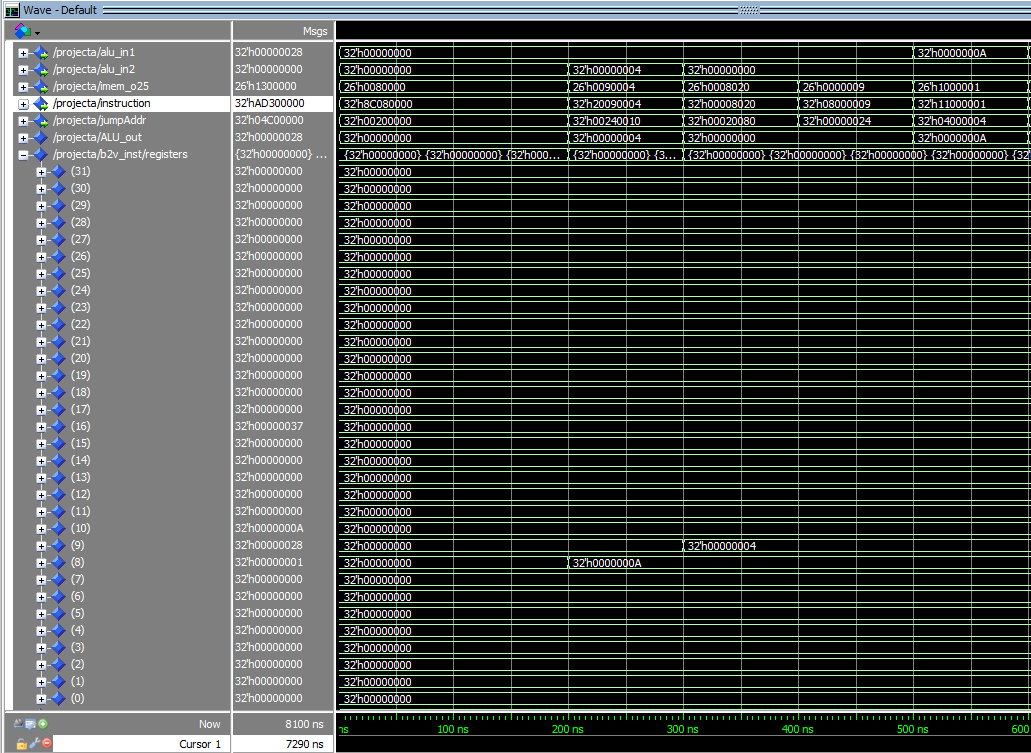
load $t0, 0($zero):



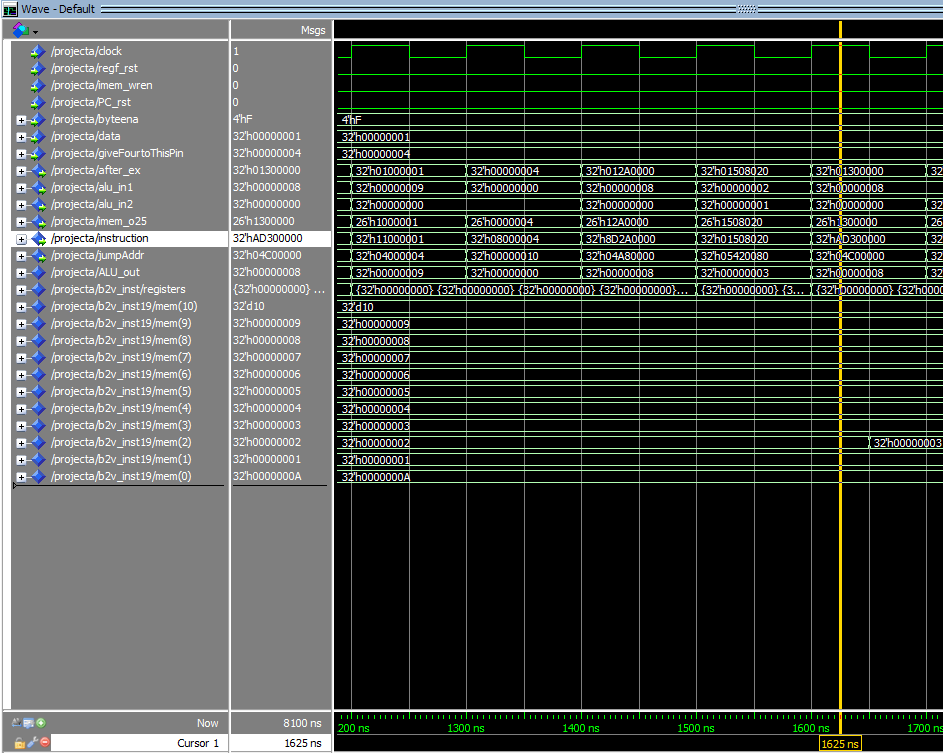
addi $t1, $zero, 4:



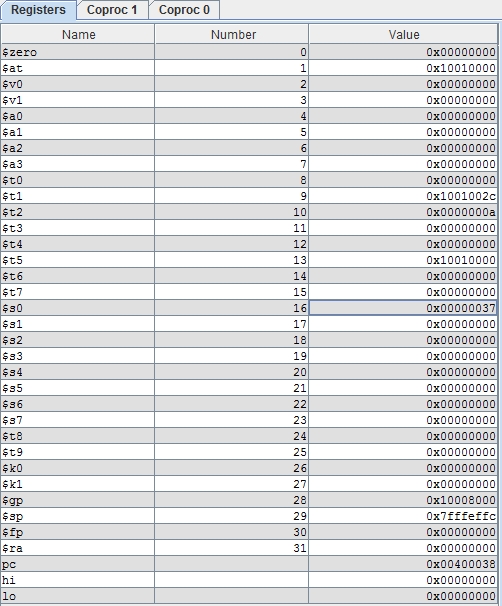
add $s0, $zero, $zero; j check:



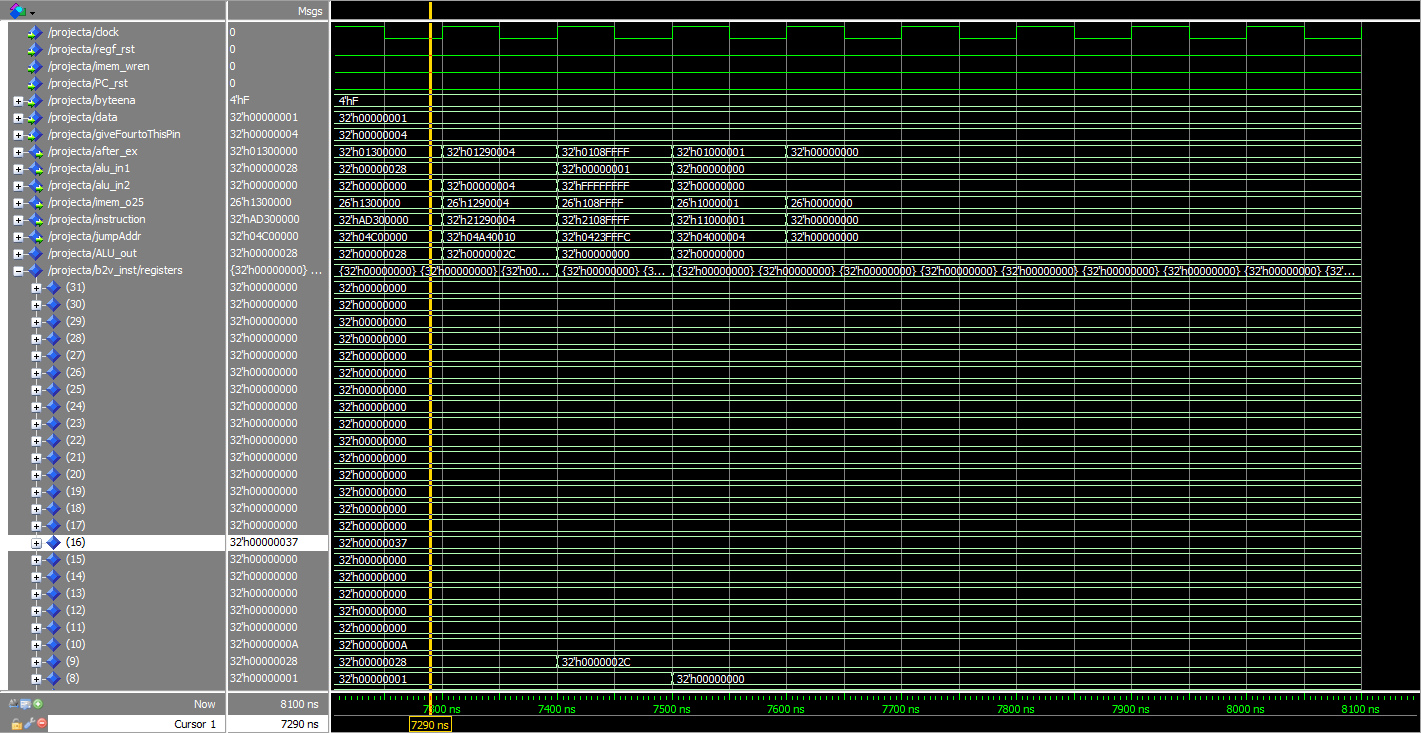
first time run sw $s0, 0($t1):

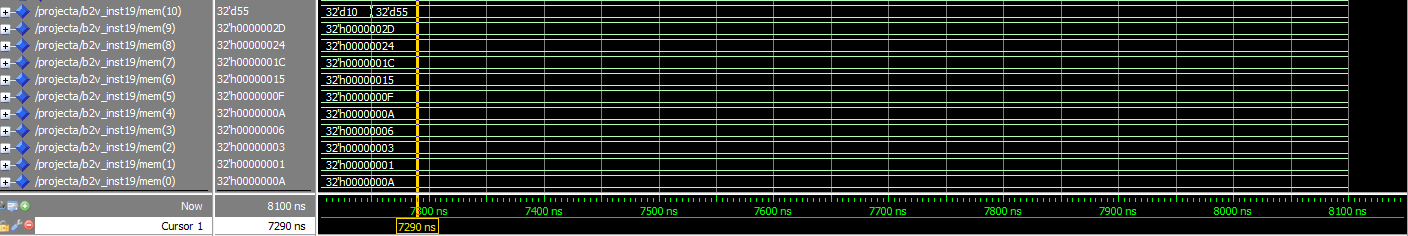


result from mars:



result in wave form:





vhdl file named projectA.vhd

during this lab I created the component jumpAddrGnrt and 26 to 32 bit extender. I also added monitoring signal outputs to monitor the values.